L Number	Hits	Search Text	DB	Time stamp
-	92325	map$4 same (method or technolog$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	59	(map$4 same (method or technolog$4)) and (divide adj block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	14780	(map$4 same (method or technolog$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	11666	((map$4 same (method or technolog$4)) and replacement) and block	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	9942	map$4 adj3 (method or technolog$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	1319	(map$4 adj3 (method or technolog$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	512	((map$4 adj3 (method or technolog$4)) and replacement) and candidate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	446	(((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	444	((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	802	map$4 adj3 technology	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	576	(map$4 adj3 technology) and portion	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:39
-	3	((map$4 same (method or technolog$4)) and (divide adj block)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	113	((map$4 same (method or technolog$4)) and replacement) and (sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	113	(((map$4 same (method or technolog$4)) and replacement) and block) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40

-	339	(map$4 same (method or technolog$4)) and (replacement near5 block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	11	(((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	29	((map$4 adj3 (method or technolog$4)) and replacement) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	148	(((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4) and optimization	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	93	(((map$4 adj3 technology) and portion) and optimiz$5) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	350	((map$4 adj3 technology) and portion) and optimiz$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:40
-	12	"6023566"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:42
-	22	"5696694"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 06:42

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040093569 A1	20040513	18	HDL timing generator	716/3
2	US 20040019857 A1	20040129	49	Method and apparatus for specifying encoded sub-networks	716/1
3	US 20030217350 A1	20031120	49	Method and apparatus for producing a circuit description of a design	716/18
4	US 20030217340 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
5	US 20030217339 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
6	US 20030159116 A1	20030821	48	Method and apparatus for specifying encoded sub-networks	716/3
7	US 20030159115 A1	20030821	48	Method and apparatus for performing technology mapping	716/3
8	US 20030154449 A1	20030814	48	Method and apparatus for performing technology mapping	716/3
9	US 20030154448 A1	20030814	48	Method and apparatus for producing a circuit description of a design	716/3
10	US 20030149945 A1	20030807	14	Method and system of data processor design	716/3
11	US 20020157063 A1	20021024	1889	Implicit mapping of technology independent network to library cells	716/1
12	US 6539536 B1	20030325	69	Electronic design automation system and methods utilizing groups of multiple cells having loop-back connections for modeling port electrical characteristics	716/18
13	US 6519757 B1	20030211	7	Hardware design language generation for input/output logic level	716/18

	Document ID	Issue Date	Pages	Title	Current OR
14	US 6496972 B1	20021217	56	Method and system for circuit design top level and block optimization	716/18
15	US 6490717 B1	20021203	32	Generation of sub-netlists for use in incremental compilation	716/18
16	US 6467077 B1	20021015	73	Capturing an evolving wafer fabrication method and system	716/19
17	US 6134705 A	20001017	32	Generation of sub-netlists for use in incremental compilation	716/18
18	US 5903466 A	19990511	37	Constraint driven insertion of scan logic for implementing design for test within an integrated circuit design	716/18
19	US 5831868 A	19981103	35	Test ready compiler for design for test synthesis	716/18
20	US 5787010 A	19980728	30	Enhanced dynamic programming method for technology mapping of combinational logic circuits	716/7
21	US 5703789 A	19971230	36	Test ready compiler for design for test synthesis	716/4
22	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan and near full scan within design for test applications	714/726
23	US 5677847 A	19971014	17	Method and apparatus for designing a module	716/1
24	US 5663892 A	19970902	12	Method of compacting layouts of semiconductor integrated circuit designed in a hierarchy	716/2
25	US 5625567 A	19970429	28	Electronic circuit design system and method with programmable addition and manipulation of logic elements surrounding terminals	716/3

	Document ID	Issue Date	Pages	Title	Current OR
26	US 5526276 A	19960611	28	Select set-based technology mapping method and apparatus	716/17
27	US 5311442 A	19940510	22	Technology mapping apparatus for a combination circuit for use in automatically synthesizing an LSI logic circuit	716/18
28	US 4751656 A	19880614	17	Method for choosing replacement lines in a two dimensionally redundant array	716/1
29	US 4703435 A	19871027	16	Logic Synthesizer	716/18